Implementable ideas to create Atmanirbhar Bharat in Telecom Chips : Fabless Telecom Chip Industry

Semiconductor Technology in India: The forgotten future

India at some point of time ignored the need to build its prowess in the semiconductor technology. Rest of the world realized that all the electronic systems are getting into Integrated Circuits and the data creation, manipulation (compute), communication, control of infrastructure and rendering to human interfaces all would be through these ICs. There have been huge strides taken by the western entrepreneurship driven ecosystems in the past 3-4 decades and by some eastern establishment driven ecosystems in the last couple of decades in this domain. While we in India have not created these, over time we have become significant consumers of all this technology. It is ironic that it was Dr J C Bose on Indian soil who invented the first communication receiver on a diode nearly 120 years back and India at this time does not own much of this technology. A billion phones, many billion gadgets, not a single our own!! While we have been smart to invest into some strategic technologies like space and atomic energy, for some reason we have failed to foresee the criticality of semiconductors that in fact are integral components of even those strategic technologies. Lack of a minimum level of capability in semiconductor technology will also hold us back in all cutting-edge technology areas like Aerospace (e.g. Drones), Artificial Intelligence, IoT, Data Sciences, Communication, Industrial automation, Transportation and even areas like Medicine and Biotechnology. It's a future we forgot to work upon. Now it is so late that without serious intervention by the establishment, we might be lost forever. In this paper we examine how a fillip can be given to this ecosystem so that this gets addressed at least in the future.

Outline:

Before going into the steps that are possible to do this, it is imperative that we look at how the rest of the world has fared in this and has come up; so that we can learn the size of the problem we are facing and maybe derive some methodologies and insights about how we can approach a catch up.

I must warn here that this discourse will contain some serious technology components referred so that a person with ordinary education in general sciences might also find tough to comprehend. I have been asked in the past to suggest the solutions in "common man parlance". While I will try my best to keep it that way, I am afraid that such an effort may be as futile as asking a common man to conduct a complicated surgery. What we need are people who can understand the technology as well as the tact and management/leadership capabilities to bring about a change.

The Western History

Over time, the western ecosystem evolved taking one step at a time. I would have to include Japan as part of this portion of history as well. An electronic system consisted of a circuit board consisting of many components and working in unison. The basic components used in such circuit board are

a. Passive components like resistors, capacitors, inductors, transformers, relays etc.
b. Active components like diodes, bipolar transistors, FETS

And we can make some of these in some primitive way in India. Over time material sciences research have made these components also very sophisticated.

At some point of time, the concept of integrating multiple such components in a silicon wafer was invented by Texas Instruments and over the decades millions and billions of components have been put in

one piece of silicon. The earlier integrated Circuits were simple. Year on year, the semiconductor companies took incremental steps and made more complex integrated circuits. This is an important factor to comprehend in the economic cycle of this evolution. It cost a private company little more to make an integrated circuit compared to an active component. They could build that and a business around that and enough R&D money to create the next integrated circuit, a little more complex. All these advances were first consumed by their own defence requirements, almost providing a guaranteed market. After a delay, others in the world consumed these. Over multiple such cycles, there were a few large companies like Intel, Texas Instruments, National Semiconductor, ST Micro that could design complex circuits and put them on one piece of silicon, i.e. fabricate the designed circuit and sell them in reasonably large numbers to sustain the next R&D cycles. As this progressed, the complexity of circuit design could not be handled by manual methods and Automated Computer Aided Design (CAD) methodologies were invented. Similarly, the fabrication and manufacturing also became sophisticated. However, the complexity and cost of both these activities started becoming much larger. So these companies started having two distinct types of activities

a. Design of complex semiconductor chips
b. Fabrication of highly integrated chips

It's almost like a newspaper company, one major activity is to gather all the necessary news, write the articles, edit them, lay them out and prepare for printing, the other activity to print it (and invest R&D on next best printing press for future).

Many semiconductor companies initially did their own CAD and automation tools. Eventually, some companies were founded to purely supply the EDA and CAD software tools to the Semiconductor companies. Also, the economics of fabrication soon became so large that keeping a fabrication setup running within a semiconductor company became unviable for most of the companies. A fab would take millions of dollars a week to just stay on. One cannot switch them off and on at will since it takes long time for a fab to switch on and reach reliable production. So, a new model of outsourced fabrication (similar to media companies outsourcing the printing) took off creating an ecosystem of companies centered around the Fabless Semiconductor Companies

a. Fabless Semiconductor Companies
b. EDA and CAD companies
c. Fabrication houses
d. Packaging and test companies
e. Semiconductor IP Companies

Once the Fabrication was outsourced, a new industry of Semiconductor IP companies that create components for the use of Fabless Semiconductor Companies came in. TSMC, Global Foundries, UMC are a couple of Fabrication Houses; Qualcomm, Broadcom, Marvell are some notable Fabless Semiconductor companies. The Fabless Semiconductor Companies focus on all the circuit design and layout of the application while the Fabrication house creates the "masks" (like the printing plates) and then mass manufactures the chips. Nearly all the new Companies in the world founded after the 1990s and selling chips are Fabless Semiconductor Companies. Interestingly again, the first company in the world founded in this manner was Cirrus Logic, a fabless semiconductor company founded in the Silicon Valley by Dr. Suhas Patil, an entrepreneur of Indian origin. On the post silicon fabrication activities, companies like ASE, Amkor, Statschippac are a few examples of the packaging and test companies.

The Eastern Foray:

While this happened between 1980s and 2000 in the west, many of the manufacturing friendly eastern countries like China, Malaysia, Singapore, Philippines, South Korea etc. attracted the Western semiconductor companies to set up their manufacturing bases in their countries. Skilled and cheap labour, productivity-oriented policies and work culture and the clear will power of the Governments of their countries made this possible. While the packaging and test activities started first, eventually with TSMC, even the semiconductor manufacturing moved into the Eastern world. However, the real ownership of chips beyond Japan was not present before the turn of the millennium, in the last 20 years, companies from Taiwan, S. Korea and China have started in the fabless model and owning chips. With a high degree of intellectual capital, India has attracted almost every company in the world to set up its design houses, exporting services. This model unfortunately does not lead to any ownership of the products in the country unless the intellectual capital decides to build Indian owned chips.

Start-up: The Big Company Effect

Let us see how the new efforts picked up in the last 40 years across the world. If we need to start catching up, we must study how the others did. The Fabless model started by Patil Systems Inc. in 1981 (Cirrus Logic) paved way for many new companies that could own a chip without having to own a fab. In the next 20 years many fabless semiconductor companies were founded. Also, the fact that each chip was small and low in complexity made it easy for companies with a decent small idea to launch business and try out their luck without burning too much money or wasting a lot of time. However, by 2000, the increasing complexity of design and the costs of outsourced fabrication in advanced technology nodes started making the semiconductor start-ups look like white elephant calves. One could no longer make a new company based on a novel component like an amplifier or a processor. A complete System on Chip had to be built. One had to invest USD 50-100Million to make a fabless semiconductor company take off. By around 2005, semiconductor funding in the Silicon Valley started drying up, the downturn in 2008 being the death nail on this. With the commoditized chips being mass produced in east Asian fabs, the industry adapted the cost of production plus margin model and drove itself to the bottom of the price pit. The enormous R&D costs could only be justified by a very few companies. The industry started drifting towards "winner takes all" model. Consequently, the last 10 years saw a continuous series of mergers and acquisitions with large companies coming together and creating larger behemoths. All these have created a massive entry barrier for anyone trying to enter the semiconductor business. The challenge is higher for companies from India which are trying to open their eyes now. Being 50 years late means one must clear a major backlog. The thing about chips is that a commercially viable product must be backward compatible many times. If you buy a 5G phone, you still want it to work on 4G/3G and even 2G networks. System on Chip is not enough anymore. Multiple Systems on Chip is the order of the day. It is very clear that strategic interest is a necessary ingredient to start now and build chips. But anyone with strategic interest cannot wait any further, the gap increases every day.

What has happened in India?

As mentioned earlier, India has been a major contributor to the design of chips owned by rest of the world. While most of Indian talent is engaged in the implementation of the chips, very few have exposure to the conceptualization phase (where technology and business ideation happens). India has significant backlog to catch up

Foreseeing the need for this, some companies like Saankhya Labs, Signalchip, Cirel have braved into this field. They have built chips under such hostile environment for chip building and have been a saving grace on an otherwise bleak history. There have been a few Indian companies building IPs for the consumption of semiconductor product companies which also find it difficult to survive due to the shrinking number of potential customers thanks to the recent consolidation.

Also, there is a misconception that owning chips means "manufacturing in India". It does not take too much of education to know that most chips in the world are owned by fabless companies. While it is important to manufacture in India, this approach is like focusing on the printing press and not bothering about the ownership of newspaper. In fact, the few chips owned by Indian fabless companies are not even considered as local contents within the policy frameworks of indigenization policies like Make in India etc.

This has had a slowing effect on focus on fabless chip ownership and has been detrimental to real chip ownership. This all or nothing thinking of "Since the ownership arises only when we manufacture, and manufacturing is a very expensive effort let us not think about fabless effort this until that is done" is like saying "Since the printing press is an expensive thing, let us import our newspapers also".

Even if a fab is built in India, as explained in the earlier sections, different types of chips will require different technology flavours that, it is unlikely that in a foreseeable future, all Indian designed chips will be manufactured in India.

What needs to be done?

1. Remove Hurdles:

   Owning a semiconductor chip is almost always through the Fabless model. This is how most chips will be created. Educate the policy makers about this. Call Chips owned by Indian Fabless companies as Local Content. Treat these chips as Indian in all respects.

   Also, many simple tasks like shipping fabricated chips, packaging etc. face extremely complicated customs/export/import restrictions that the founders are mostly spending time breaking their heads over finding out clean ways to send courier etc. Please see Annex A for detailed explanation and suggestions on specific solutions to this issue.

2. Use the platform already built: Help existing few to survive and take the next steps

   The existing companies have created some remarkable chips by somehow sticking to it and innovating around the barriers. Saankhya has augmented its chips with system business to reach revenues. Signalchip is trying to innovate around Moore's law to create chips at low development cost. WiSig is making chips for IoT in collaboration with academic institute IITH. Almost all these companies have founders and dedicated employees that work at a fraction of their market salaries to keep the story on. However, they have created multiple systems on chip that are world class. They have covered the backlogs in some fields. It is important that we utilize this platform and help these companies take the next steps. These companies can now take up development in strategic areas like 5G, SDR etc. Adding 5G chip development by private industry as part of the 5G testbed project and providing them with some R&D grants to speed up the development would be the best win-win outcome at this time.

3. Understand and acknowledge the real costs involved

Chip design is not cheap, not even close to it. While it is not as expensive as setting up a fab, it is still seriously expensive. It is important to understand the amount of money needed to design and bring a chip into market if we need to do anything about it. Even with Indian "inexpensive talent", chip design is costly. The following table summarizes an indicative cost of R&D for development of chips in 40nm node. The newer competitive nodes will be more expensive.

Type of chip	Examples	Indicative R&D Cost (INR)
Small Single Function	GNSS, IOT end point	25Cr-35Cr
Medium Size	Low end WiFi, Wireless Transceiver	50Cr-70Cr
Typical SoC	Modem, SDR	120-150Cr
Large SoC	Compute Processor	200Cr -250Cr

The following chart shows the relative expenses of a typical chip development

Any incentive program needs to keep this quantum in mind. Typical development cycles from inception to market readiness are two to four years.

4. Making the economics work

Let us take a chip development activity costing 20Million $. Even if the Government is ready to help 50% of this amount, it would be difficult to find entrepreneurs and investors risking 10M$ on a chip idea these days. Commoditization is a major challenge chip companies face. Many chips we use have been selling in huge volumes that the prices have become commoditized. Chips have become commoditized leading to the following paradigms…

- Extreme investment to make cheap chips
- High value for company, low value for chips
- Poor business case unless a company can be sure of millions of chips if this

is the case,

- What is the motivation for investors to invest into chips in India?
- Left to its own, this industry will not take off in a poor nation like ours
- Will we ever be "ATMANIRBHAR" (do we need to be)?

While this chip price is a market dynamic (which seems to be correcting a little in the 2020-22), many large software corporations and countries have understood the strategic importance of owning the technology at core level and started building their own chips. In fact, due to this disparity present in the general semiconductor industry, even the worldwide chip design activities are now happening within

larger software giants like Amazon, Google, Microsoft etc. Large OEMs like Apple and Samsung also do their own chip design. They do this strategically since there is a larger gain seen elsewhere in their business. For example, Google did an AI chip so that its expenses on its servers were reduced significantly.

India uses billions of chips, especially in telecom. Day to day life, economy, security, "rozi roti" of billions depends on chips. As a country, India has a lot of strategic requirements for owning a bunch of semiconductor chips. In fact, when aggregated at the level of the entire nation, even the economics work out very well. We will need to convert these national level strategic requirement and economic opportunity into a business opportunity for Indian Industry to make new people venture into this field.

5. Help new companies to come up

Today, the chips getting funded in the international VC funding area are very high-end ones for AI/ML and data centers. But from a security perspective, there are a whole lot of chips that we use currently on which it would make sense to have Indian ownership but might not be viable for a new company to sell its business plan to investors and itself. As an example, a lot of data in India moves on Wi-Fi chips. Wi-Fi chips sell at <3$ apiece. Assume an investment of 10-15M$ on this chip, it would take a sale of more than 10M units to make ROI assuming a 1$ margin. It would be very difficult for a VC to make investment on this business plan. Even the founders will shy away. But this technology is ubiquitous and newer versions of these standards for Wi-Fi will keep coming, new chips will be made by the incumbents at incremental costs, and we will keep using them for long time. The gap will grow further making it more difficult to justify a later catch-up activity. As a country there is a strategic need. If this can be presented as a business opportunity to the Indian companies, a couple of them might develop them with the hope that the IP would be useful for future chips. Subsidizing the sale of chips by Indian companies is another method. It is important to ensure that chips incentivized thus are going to be competitive in the global market from a definition, quality and performance perspective, so that once the catch-up is over, they sustain in the free market.

6. Encourage/incentivize top talent to work in Indian MSMEs.

Chip design is a highly specialized effort and requires some of the best engineering talent to work on it. Largest expense faced by R&D oriented activity like chip design is paying top talent that choose to join high paying jobs. The MSME/start-ups find it difficult to hire top talent and retain them. It is important to incentivize the top talent to work in R&D oriented deep tech start-ups/MSMEs

7. Do not Penalize genuine efforts:

One of the features of many programs is extreme penalties in case of failure. Fear of failure is the single most reason why people don't try new things. Especially when the target is long term and markets are uncertain, the fear factor is already high. While checks and balances are needed to make sure proper usage of the funds, GoI should not penalize genuine failures (especially for not being able to perform things that companies don't have direct control, like market success).

Specific steps: How to get back on track

1. Call Indian chips Indian:

a. Correct the PLI, Preferred Market Access polices across the board to reflect that Chips owned by Indian Fabless companies as Local Content, irrespective of where they are manufactured.

b. Public Procurement Notification has no additional weightage for using chips designed in India in local content calculation. Provide additional weightage for chips owned by Indian companies.

c. Promote Indian core technology, example: additional weightage for using IRNSS where any GNSS is required.

d. Recognize chips owned by Indian Fables Companies as "Made in India". Policy changes to recognize the chips sold by such companies to customers in other countries as exports (even though fabricated in other parts of the world).

2. Clear the existing hurdles for operating across trusted nations:

a. Ease the duties and complex mechanisms of import/export of wafers/dice/packaged chips/test boards by Fabless Indian Companies

b. A detailed description of the problem and some suggestions are presented in Annex A

3. Treat Private R&D equal to academic R&D

a. Trust the private companies

b. ROI will be realized through rupee saved in import substitution and increased exports

c. Extremely deep R&D needs some serious backing.

d. A mechanism to include bona-fide in-house R&D in Indian start-ups, MSMEs into the R&D support schemes that are available to academia are presented in Annex B.

4. Identify different kinds of chips of national interest and support their development in the appropriate manner

A. CHIPS FOR CRITICAL/STRATEGIC INFRASTRUCTURE

a. Networks for National Security, defence

b. Networks for internal security, law and order

c. National Telecom Network on which Govt. Machinery runs

d. Networks for hazard/health/disaster management

e. These are the chips that are necessary for the country to have in its ownership. Government (Defence, DPSU, PSU) would be a customer for these chips.

e.i. Chips that are used in defense equipment

e.ii. Chips that carry Govt and strategic data

e.iii. Chips whose non-availability can cause a serious loss to the country

f. If a chip needed for these is present in India, make it mandatory that it is used in developing systems for these purposes

g. If such a chip is not present in the hands of an Indian company, call for Indian companies to develop the chips for these and supply to Govt/DPSU (insist on IP level ownership in India). Chip Design challenge is a good way to get this going (detailed in Annex C)

h. This activity itself will allow some companies to find some footing.

i. Many large corporations in the world today started off their journey this way

B. GENERIC REPLACEMENT CHIPS

a. Generic chips (like discrete, ADCs, DACs, amplifiers etc.) present in existing systems made by DPSUs/PSUs

b. Can be replaced by Indian Chips to increase local content

c. Fund the development of some generic replacement chips for systems on which we need complete ownership. Such chips might not have useful commercial value outside the strategic need. But will again help the Companies find footing and larger number of small ideas can be accommodated from many companies, paving way for an ecosystem.

C. COMMERCIAL CHIPS FOR UBIQUITOUS QUINTESSENTIAL USAGE BY COMMON MAN

a. Commodity Voice, Data, Video

b. Help MSME to break the backlog barriers by incentivizing private R&D on commercial chips (i.e chips that are not necessarily strategic)

b.i. Provide Grants to cover third party expenses like tape out, EDA tool licenses, Test equipment and Automated test equipment

b.ii. Reimburse 50% R&D expense

b.iii. Both on the condition that the company is Indian and any acquisition by foreign entity would require repayment of the assistance and/or a license to use the R&D within India, commensurate to the incentive received by the MSME

c. Provide a subsidy for first 1 million chips of any kind sold by an Indian company. This will help in breaking the commoditization issue.

d. Mandate usage of chips owned by Fabless Indian companies in systems claiming Make in India benefits.

e.

D. COMMERCIAL FUTURISTIC CHIPS OF HIGH PERCEIVED VALUE

a. Like AI, ML, High Performance Computing, Data Center…
b. VCs will be interested in these ideas
c. Facilitate initial seed funds, Prototypes
d. Ensure Indian companies remain Indian

5. Help Indian chip companies to build their labs

a. Provide customs waiver for lab equipment import by start-ups/MSMEs

b. The labs to test these chips need a lot of high-end equipment. There is a large availability of used high end equipment in the world. However, the import of such equipment requires special permissions and is long a drawn process due to fear of e-waste dumping. This puts a burden on the already cash starved start-ups/MSMEs to resort to buying brand-new equipment at significantly higher costs.

c. Enable import of used lab equipment by Fabless start-ups/MSMEs. A check can be implemented saying that the cost of such import shall be more than Rs 1000 per kg, which will avoid e-waste dumping.

6. Build the advanced test ecosystem: These are the tasks that are used sporadically by companies. Currently many of these require going out of the country. Common facilities for such activities will significantly help

a. Failure analysis lab

b. Telecom test lab (protocol testers etc.) given free of cost to MSME for indigenous products testing. Charged to bigger/services companies.

c. Field test and interop lab

7. Identify/Tie up with “trusted fabs”
   Identify a list of trusted fabrication houses and ensure that the chips being built with incentives above are fabricated in those fabs.

8. Come up with a scheme like STPI to encourage top talent to work in deep tech start-ups and MSMEs. One suggestion is to provide income tax holiday for employees of Indian start- ups/MSMEs working on core deep technology development for one window of 10 years in their life cycle. This will help Indian MSMEs to hire the best talent with a direct mark up of 30% on salaries of top talent in the country. Once the objective is achieved, this scheme can be sunset.

CONDITIONAL ROYALTY MODEL :

The model suggested is that Govt funds the R&D for the chip challenge winners up to a stipulated amount and upto 50% of R&D expenditure which enables the company to take the risk and spend its own

time/money to make the chips. Some of this can be upfront, some as R&D expense reimbursement. One avenue could be to fund VLSI/Chip development under TRDF. TRDF funding is generally as soft loans or grants in exceptional cases. As mentioned earlier, the break-even point for chip companies is very long term. A company would take loans if they were confident of returning the money soon enough. While soft loans are a help, Fabless will need grants. For the reasons given above, we suggest that Fabless VLSI/Chip development should be considered exceptional case and given funding as Conditional Grants.

There would be periodic reviews of the technical progress and funding can be milestone based further funding can be only to programs that show serious commitment. The model in brief:

a. Govt helps the fabless industry take the risk by funding through grants
b. Govt asks back the money when the company has it

Once the chips are in sales phase, the companies provide the Govt with a royalty. The royalty will stop once the Govt recovers the money.

What happens if no sales happen?

In case of tech performance failure, the grants would have stopped in early stage without much loss to the Govt.. Only companies that have shown tech performance would have gotten all the funding. If a technically competent product does not get market success, even the company that co-invested loses its investment. That is the risk GoI should be ready to take to develop this industry. Even in this case, Govt wins since we would definitely have become Atmanirbhar.

Can Fake companies not game this?

50% borne by the company is still a huge amount in the chip design world. It is very unlikely that a company would invest hundreds of crores to just game the system. Nevertheless, checks and balances have to be established to curb misuse of the scheme.

Annex A : Removing hurdles faced by Indian Semiconductor Companies in manufacturing/packaging of Semiconductor Chips and bringing them into India

Fabless Semiconductor companies are envisaged to form a very important part of Atmanirbhar Bharat. For the manufacture of ICs, Indian fabless companies are dependent on semiconductor fabricators (fab), who are present outside India. As part of the fabrication (manufacturing) process, the fab creates mask set specific to the particular IC. This mask set is used further to produce the actual semiconductor wafers. Semiconductor chips are created using these wafers and further they need to be packaged[1] before being sent to the Fabless Company or to its customers (who may be in India or elsewhere in the World).

While the wafer is created in a fab in one foreign country, the wafer further needs to be sent from one foreign country to another based on the availability of vendors for package encapsulation. During the package encapsulation, original wafers will be cut into hundreds/thousands of ICs and each is encapsulated with the packaging material which is separately prepared. Wafer and/or chip level testing of each chip will be done using Automated Test Equipment (ATE).

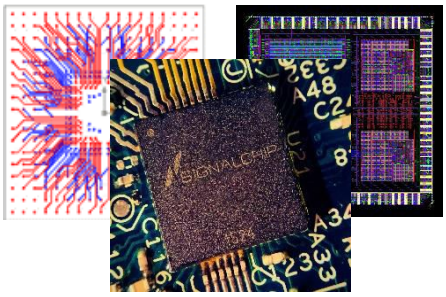
As the encapsulation involves multiple foreign vendors in different countries often there will be 2 to 3 remittances to different vendors and involves more than one Invoice. The remittances can be one-time or upfront and per wafer/chip/package cost. Final goods come in different quantities than the quantity mentioned in the first vendor's Invoice. This creates issues with the Customs clearance as Customs want the quantities to be matched with every Invoice remitted and product physically identified. But the product can be identified only with the last processing invoice. Also, physically opening wafers and half processed chips will render them unusable.

As can be seen, while the Fabless Semiconductor Company owns the design and Chip itself, the process of manufacturing it goes through multiple material procurements in more than one country. There are multiple foreign remittances needed to facilitate these activities and many compliance steps need to be followed. In some cases, the guidelines are confusing and subjective. A simple courier task becomes a massive compliance exercise every time a company must make even a test chip. There is a need to simplify the process and facilitate the smooth operation of semiconductor companies in India

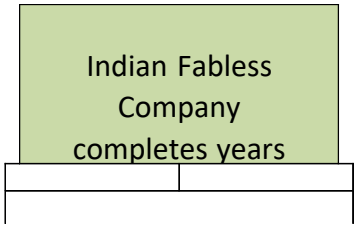
[1] Semiconductor Packaging is a specific manufacturing process and should not be confused with the general term "packing" which done for any product. Semiconductor packaging involves putting together the bare wafer dice with additional material, circuitry components, substrates, lead frames, pins and mechanical stabilizers to create the final form in which a chip is brought out to market. Such "packaged" chips will be

then “packed” in different forms like trays, tapes, reels etc. and sealed in electrostatic discharge safe pouches and shipped.

. The following figure shows the steps that fabless companies go through to manufacture either test chips or production chips.



The following flow chart describes the same in terms of the financial, invoicing/billing/filing procedures that an Indian fabless company has to follow to manufacture either test chips or production chips. The green boxes show the flow chart and the red boxes show the compliance issues they face in particular steps.



Given the lacuna in the indigenous ownership of semiconductor all this contributes to loss of money, manpower and precious time delaying progress of the country in the larger sense.

Here are some suggestions to facilitate Fabless Semiconductor Industry

b.1. Automatic Bill of Entry Waiver for remittances made to fabs in trusted countries for the purpose of mask-sets

b.2. Single Bill of Entry for package and wafer invoices when packaged chips arrive at the ports

b.3. Facilitate green channel customs clearance for bonafide Fabless semiconductor companies. Avoid physical opening of delicate semiconductor material at customs ports.

b.4. Allow Indian fabless companies to move their test equipment/PCBs at the location of testing/mass manufacturing for the duration of manufacturing without double/triple payment of customs/duties.

b.5. Recognize chips owned by Indian Fables Companies as “Made in India”. Policy changes to recognize the chips sold by such companies to customers in other countries as exports.

Annex B: R&D Grants for Fabless Telecom Chip Companies with safeguards ensuring that the IPR ownership remains within India

1. Introduction

This document briefly outlines key policy suggestions to provide support to indigenous semiconductor industry. Semiconductor's chipset are the heart and soul of technology, they define what technology products and solutions can or cannot do. Globally the semiconductor industry is dominated by large MNCs from a handful of countries, but there is a nascent indigenous industry which is doing its best to establish a foothold in this market. A little bit of policy support can go a long way in ensuring that we have a sustainable indigenous capability in this crucial domain.

The criteria outlined below were used to ensure the interests of all stake holders involved from the Government of India to public and private sector companies.

- Clear and objective criteria to qualify for support
- Well defined obligations for all stake holders, including safeguards
- Well defined outcome promoting indigenous capability

The support suggestions directly address the following main barriers

- High cost of Electronic Design Automation (EDA) tool licenses
- High cost of fabrication of the chipset in foundries (tape-out)
- High cost of productization of the chipset post silicon (ATE and Production Test development)
- High cost and limited availability of skilled labor and know-how involved in designing semiconductor IPs

Due to the nascent state of the industry and risks involved, the large initial investments required are difficult to commercially justify. One avenue could be to fund VLSI/Chip development under TRDF. TRDF funding is generally as soft loans or grants in exceptional cases. As mentioned earlier, the break- even point for chip companies is very long term. A company would take loans if they are confident of returning the money soon enough. While soft loans are definitely a help, Fabless will need grants. For the reasons given above, we suggest that VLSI/Chip development should be considered exceptional and given funding as Conditional Grants. The Grant amount may be recovered after the initial support phase through royalties on sales.

2. Support for EDA tool license

Qualification criteria	1) EDA tool licenses taken to develop and tape-out semiconductor ICs and 2) Taped-out semiconductor ICs fully owned by Indian MSME, i.e. revenue from sale of the ICs will accrue to entity registered as company in India
Nature of support	50% of cost of EDA tool licenses purchased, supported by invoices

Safeguards	Support amount paid out upon utilization for development of indigenous chips Service companies need to maintain the R&D related expenses separately (ensured by the approved R&D center requirement above)
Outcome	Creation of indigenously owned semiconductor ICs in the ICT domain Control over the core security and services of defense, strategic services and ICT enabled economy Reduction of imports, promotion of value-added exports

3. Support for chipset fabrication

Qualification criteria	1) Tape-out of semiconductor ICs fully owned by Indian MSME, i.e. revenue from sale of the ICs will accrue to entity registered as company in India 2) The development of the IC happens inside an R&D center approved by DSIR
Nature of support	50% of cost of tape-out, supported by invoices as R&D grant
Safeguards	Support amount paid out upon successful completion of tape-out
Outcome	Creation of indigenously owned semiconductor ICs in the ICT domain. Control over the core security and services of defense, strategic services and ICT enabled economy Reduction of imports, promotion of value-added exports

4. Support for ATE and Production Test Development

Qualification criteria	1) Tape-out of semiconductor ICs fully owned by Indian MSME, i.e. revenue from sale of the ICs will accrue to entity registered as company in India 2) The development of the IC happens inside an R&D center approved by DSIR
Nature of support	50% of cost of ATE development, PCBs, test floor expenses for R&D, supported by invoices as R&D grant
Safeguards	Support amount paid out upon successful completion of ATE test
Outcome	Enables the Indian Telecom Chips to move to mass production Reduction of imports, promotion of value-added exports

5. Support for semiconductor IP creation

	2) The development of the IC happens inside an R&D center approved by DSIR
Nature of support	R&D grants upto 50% of the expenses towards development and testing of core IP in the ICT domain.
Safe guards	If the IP ceases to be fully owned by Indian company, a non-exclusive license of the IP created will be automatically awarded to GoI/designated PSU. Nature of the license granted A. Architecture license: if the grant is >= 50% of the market value of the architecture license of same IP B. Multiple use source: if the grant is >= 50% of the market value of the multiple use source license of same IP C. Multiple use hard/encrypted IP license: if the grant is >= 50% of the market value of the multiple use hard/encrypted license of same IP D. Single use source: if the grant is >= 50% of the market value of the single use source license of same IP E. Single use hard/encrypted IP license: if the grant is >= 50% of the market value of the single use hard/encrypted license of same IP Market value to be determined by a committee of representatives from the industry and GoI/PSU/Academia/Market Research
Outcome	Creation of library of indigenously owned semiconductor IPs leading to a multitude of indigenous chips in the longer run

Annex C: Telecom Chip Design Challenge

As outlined earlier in this document, there are certain chips that are critical for the strategic telecom networks in the country. Today, telecom equipment makers find it difficult to make systems with core Indian content since there aren't many Indian chips for their data paths. While there are a few Indian Chip design companies with capability and chips to address some of the requirements, they need market visibility and funding support to hasten their development of 5G RAN chips. A chip design grant challenge would serve both the purposes very effectively.

The suggestion here is to identify three-four specific chips that are relevant today and throw open a grant challenge to the existing companies in the country to develop them. The advent of 5G provides an excellent opportunity to do this. 1-2 companies can be selected to develop each chip using grants.
The grants can be for chips targeting

a. 5G Radio Unit
b. 5G Distributed Unit and Central Unit
c. Small Cells
d. NBIoT
e. SDR
f. Power Amplifiers
g. UE, i.e. mobiles

A fair selection procedure can be used to pick 1-2 companies to execute each of the chosen chips. At the end of this effort, we will have a healthy set of chips that can fuel the RAN equipment in India and elsewhere. With this, a truly Atmanirbhar 5G can be created in a 2-3 year horizon.

Checks and balances mentioned in Annex B can be brought into the scope to ensure that Indian IPR remains Indian and the benefits go to Indian companies.